

Logic Style Comparison for Ultra Low Power Applications

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Abstract—Power consumption factors such as leakage and device capacitance are inherently dependent on the type of logic family chosen to implement an application. This work compares the suitability of static CMOS, DPL, DVL, CPL and pseudo-nMOS logic families for use in near-threshold supply voltage environments. Through the joint analysis of addition logic and a register, we show a combination of CMOS and passgates performs best in terms of energy. The results of this analysis also demonstrate how the optimum supply voltage varies with logic styles in ultra low power systems.

I. INTRODUCTION

Several investigations of digital circuit logic have been proposed recently for ultra-low voltage operation [1][2][3][4]. In this work we compare the various logic styles within an ultra low-voltage range. The analysis of classic simple gates only [3][4] is not representative of the actual trade-offs inherent to each logic family since a single gate performance is dependent on the setup. A global system [1][2] does show how a certain logic style performs but lacks the comparative analysis. Therefore, a unified aspect on general logic and ultra-low voltage design characteristics is presented in this work to overcome these limitations.

II. DIGITAL CIRCUIT LOGIC STYLES

At nominal voltage a trade off between energy and speed already exists for the various logic styles available. Using ultra low voltage implies this trade off is biased towards energy minimization. In this section we analyze the representative logic styles and select only the ones with the potential application for ultra low voltage operation.

A. Voltage-Restricted Logic Styles

The voltage drop due to the threshold voltage (V_T) of MOS transistors can be an important feature in some logic styles. In CPL (Complementary Passgate Logic) logic, the level high of the logic tree is $V_{dd}-V_t$ since the trees are made of nMOS transistors only. Its output is buffered with an inverter to bring the level high to V_{dd} . Hence the level high

before the inverter must be greater than $V_{dd}/2$ so that the inverter buffer can actually amplify the level high instead of attenuate it. This explains why CPL can only operate for V_{dd} greater than twice V_t . Recent work has been done on XOR logic gates and full-adders [6][7] with limited number of transistors. However all of these circuits are based on saving redundant paths by allowing internal nodes to be at $V_{dd}-V_t$ at logic level high. This means none of these logic styles can be used at voltages approaching $V_{dd}=2V_t$ or below.

Pseudo-nMOS logic also has a restricted voltage swing, but for a different reason: the pMOS ensuring the level high when the path to ground is off is constantly turned on. However when the path to ground is on, the pMOS resistance may be comparable to the nMOS path resistance. This typically yields several undesirable effects: a level low voltage not at ground level, a constant current consumption and nMOS transistors oversized to reduce the resistance of the path to ground. This last effect implies larger gate capacitances. Pseudo-nMOS has been proposed [4] by claiming this logic style presents better voltage transfer characteristic at low voltage and lesser transistors per gate hence achieving best PDP (Power Delay Product). However, in this study our primary target is to achieve lowest energy and the PDP metric does not apply in this analysis. Furthermore, ratioed logic such as pseudo-nMOS yields a high static power which prevents the circuits to achieve minimum energy consumption. And, the benefit of the limited number of transistors is offset by the increase in gate capacitance to reduce the resistance of the path to ground.

B. Static Full Rail Logic Styles

CMOS static, DPL (Dual Passgate Logic) and DVL (Dual Value Logic) are commonly used as low power logic circuit styles [1][2][3][5]. Classic static CMOS has proved to be functional and efficient at ultra low voltage [2] even though the pMOS logic tree is redundant and increases the total amount of switched capacitance per gate. DPL also has similar characteristics and is usually included within static CMOS standard cells as it efficiently implements the MUX

and XOR type functions. This logic style combination is referred to as a separate logic style, CMOS+ [3]. DVL is based on DPL logic and relies on the simplification of the redundant paths with a careful synthesis methodology [5]. Although this logic style is based on pass-transistors, DVL remains a full rail logic style. This means none of the internal nodes need to be buffered and this property makes this logic a potential candidate for ultra low voltage operation. However, the major issue in passgate logic synthesis is the irregular nature of the input capacitances within a single gate. Both DPL and DVL present the problem of long device stacks or chains during synthesis. The common solution is to buffer all the drain or source inputs with inverters for every cell [1][3]. Unfortunately, this leads to less efficient designs due to the overhead of all the inverters [2].

III. CONTEXT ANALYSIS

When a specific function is implemented with a given logic style, the performance in term of energy and delay are dependent on the logic style of the block itself but also on the logic style of blocks connected to it. Mixing logic styles between blocks can lead towards less efficient overall designs: For example, if a dual rail logic block is driven by a single rail logic block; additional inverters have to be introduced. This induces a delay bias between true and complement inputs and can increase short circuit power within the dual rail logic block (e.g. DCVS). Such effects can make the dual rail logic less appealing than the single rail logic in term of power consumption. However, within a logic cell or a complex gate, mixing logic styles can improve performance. For example, it is clear that passgate logic implements MUX and XOR type functions more efficiently than static CMOS and, inversely static CMOS is very efficient for basic inverting gates such as AOI, OAI, NAND. Hence building a logic tree that needs both types of gates can be implemented more efficiently with both logic styles combined than with one logic style only. Consequently comparing single gate implementations for the purpose of logic style comparison is misleading. This increases the complexity of standard cells and synthesis tools which tend to standardize cell interfaces, hence limiting most of the circuit optimization. Even though combinations of static CMOS and DPL have been proposed (CMOS+, [3]) the benefit is not as clear since the Input/Output standardization process introduces additional inverters. At nominal voltage operation these standard cells yield good enough results for the time to market constraint. However in the ultra low voltage operation area, variations in energy consumption are more sensitive to implementation details and standardized practices such as additional inverters or stack restriction [2]. For the purpose of logic style comparison, it is therefore necessary to compare common logic blocks with various implementations rather than just the gates. For this work, we use the classic ripple carry adder block since addition structure comparison is beyond the scope of this work and may alter the comparison.

IV. LOGIC AND TOPOLOGIES

As described in section II, voltage restricted logic style cannot yield minimal energy comparable to full rail logic styles when voltage is reduced towards sub-threshold supply voltage. By evaluating the ripple carry adder we restrict the analysis to the FA (full adder). This particular circuit represents mostly the performance of the XOR and MUX functions. But still, evaluating the energy performance of the full adder by itself may be misleading because of the tight dependence between a gate and the setup which does not take in account glitching and input switching activity [3]. we chose the typical ultra low power adder topology, a 16bit ripple carry adder to overcome this issue. The implementation of a FA cell in CMOS+ is based on the principle from [8]. For the DVL implementation, both true and complement of the carry-in are needed at every bit. Consequently for the implementation of the DVL ripple adder the carry must be inverted [8]. This makes sure that there are no pass transistor connections from cell to cell. Since the number of transistors of the DVL implementation is a subset of the DPL one with the same full rail output characteristic, the DPL cannot achieve lower energy consumption [5]. Note that the CMOS+ implementation of the FA is done with passgates and inverters only. This type of implementation is equivalent to a two stage DPL or DVL implementation because the 2 inputs XOR and MUX functions are the same in DPL, DVL and CMOS+. For the static CMOS circuit we use the classic version of the FA. The input inverters of both CMOS+ and DVL are optional and depend on the simulation setup as explained in the next section.

V. SIMULATION SETUP

The H-SPICE simulations are done with a nominal 130nm process targeted for low leakage applications. The SPICE models are derived from factory devices and provide a continuous relationship between sub-threshold and above threshold operation. DIBL (Drain Induced Barrier Lowering) effect is also included.

A. Energy components and assumptions

An important device mechanism (DIBL) can modify a digital design strategy due to its relationship with leakage [9]. Figure 1 shows the benefit of stacking transistors as a function of supply voltage. Going to a stack of one (Reference) instead of two transistors incurs a 13x increase in leakage at nominal voltage which changes to 3x only at 300mv. This partly explains the global increase of the leakage portion of the energy spent when the supply voltage is reduced. The other important mechanism that leads to increased leakage at ultra low voltage is the voltage divider effect [1]. As voltage is reduced and gets closer to V_T , the ON path resistance becomes non-negligible versus the OFF path resistance resulting in a non full rail swing regardless of the logic style. This DC voltage offset impacts the next stage and propagates the effect further. Eventually, when operating at voltages far below V_T this effect gets amplified and the

resistances of the ON and OFF paths become equal, causing circuit failure.

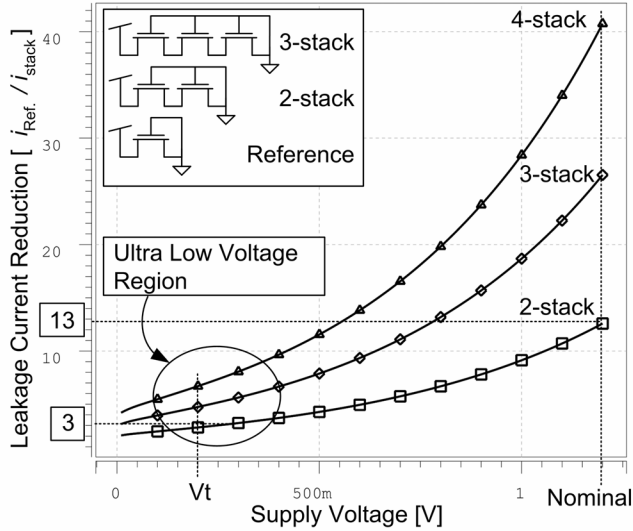


Figure 1: Stack effect (DIBL) influence on leakage when dependency with voltage is taken in account.

B. Logic Function Simulation and test bench

In order to evaluate the energy consumption of an adder we applied 50 random vectors sequentially to the structure. This takes into account the internal switching activity properly, and most importantly, all the random glitching that happens between computations. These effects have to be taken into account since the leakage component of energy consumption is greater at ultra low voltage. This increased leakage induces slower transition times because the OFF path does not get switched off all the way, hence amplifying glitching effects. we observe that only a 5% variation in energy is observed between a 50 and a 100 vector run. In all cases the delay reported is for the critical path.

A problem arises from comparing logic that uses true and complement inputs versus single inputs such as simple static CMOS. If we consider the Master-Slave latch as a classic CSE(Clock Storage Elements) used for low power systems [10], and ultra low voltage operation [11] and the adder is driven by a register. The inclusion of the complementing input inverter energies is unfair when speed is of no concern. In the MS-latch both Q and Qb are available since the feedback inverter of the slave stage is required. Consequently including another inverter in the FA is not necessary. However, connecting both Q and Qb increases the energy usage of the CSE. Typically, this option yields worse results at nominal voltage because the energy loss from switching capacitance when upsizing the CSE is not worth the saving of one inverter. In our case, at near threshold voltage, switching capacitance is less of a concern because all transistors are minimum size and leakage energy is not negligible. Since the inverter is a one-stack gate, it is one of the leakiest components and removing it can be advantageous at ultra low voltage. However, parallel leakage

and sneak leakage effect [1] appear the usage of inverters may be required. For this work, we evaluated the MS-Latch [10] energy delay performance at the optimum setup time [12] with scaled voltages and frequencies to match the circuit configuration attached to it.

VI. RESULTS

A. Logic behavior

Figure 2 shows the results for the various logic styles analyzed for the adder. We show the results for the full adder chain in the following logic styles under their best conditions: single stage DVL without input inverters, static CMOS and CMOS+ (or two stages DVL) without input inverters. DPL, Pseudo-nMOS and CPL are not shown since they cannot achieve lower power than DVL and CMOS as explained in section II and IV. Figure 2 shows the single stage DVL performs worse than CMOS for all voltages and the minimum energy is achieved for a voltage supply of 300mV. For both CMOS and CMOS+ the optimum voltage is 270mV which remains above threshold (220mV). In the best design conditions, meaning true and complement are always available, CMOS+ performs best. However,

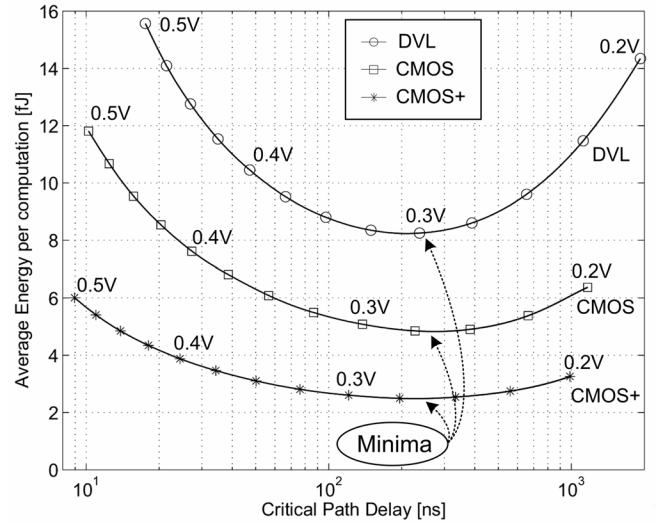


Figure 2: Energy-Delay characteristic of a 16 bit Full Adder chain depending on the logic styles.

B. CSE impact on logic style

For the purpose of evaluating the impact of dual input logic styles such as CMOS+, we examine in this section the Energy-Delay characteristic of the PowerPC master slave latch under two different loading conditions: when Q only is loaded and when both Q & Qb are loaded. Figure 3(a) shows the variations in delay and energy between the two options for a 16 bit register. Note that the cost in energy and delay for loading both Q & Qb instead of Q only remains relatively constant as voltage is scaled down: From 0.5V to 0.2V the energy cost varies respectively from 6% to 4% and the delay cost varies respectively from 40% to 30%.

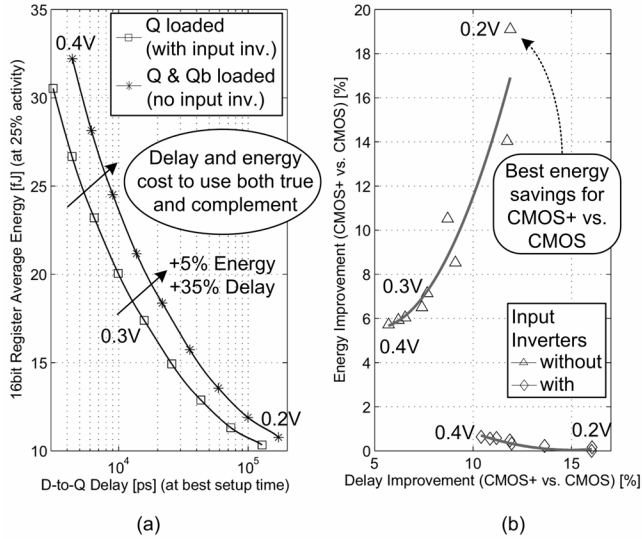


Figure 3: Energy-Delay curve of a 16 bit register under two loading conditions (a), impact of the loading on the ED improvement of CMOS+ versus classic CMOS (b).

C. Comparison Results

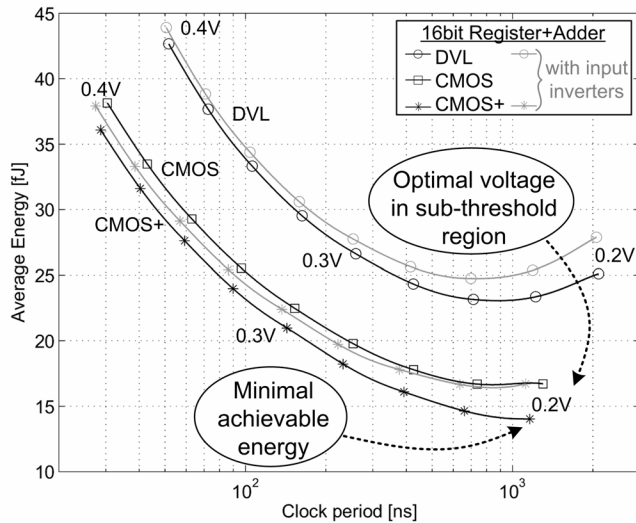


Figure 4: ED curves of 1 register and 1 adder combination for several logic styles.

For the ripple carry adder, when the input inverters are included they can increase the energy up to 2x. Hence, when their energy is included the minimum energy attainable is equal to simple CMOS. Consequently, if the previous stage provides both true and complements CMOS+ yield minimum energy. Since the register Energy-Delay behavior differs from the logic alone, before deciding the type of logic to use in an ultra low power / ultra low voltage system the architect must carefully account for the amount of registers versus logic in the system. It is clear from Figure 2 and 3 a single register is at least twice the energy of the simplest adder. Consequently if we combine one register and one adder as shown in Figure 4 the optimum voltage shifts downwards. This means the impact of the CSE is

significant enough to push the operating point of the logic towards a less efficient zone. Figure 4 which combines a register and an adder proposes to use a voltage of 200mV while the adder itself (Figure 2) suggests an optimum voltage of 270mV. Additionally, in Figure 3(b) we show the improvement of CMOS+ or two stages DVL full adders versus the classic CMOS implementation. As voltage decreases to the optimum value (200mV) the savings in energy reach up to 20% when the input buffers are removed and the FA is using the inverter from the slave stage of the MS-Latch.

VII. CONCLUSION

This work shows the combination of static CMOS and passgates, also referred as CMOS+, yield minimum energy at ultra low voltage. Additionally, by taking in account the features of the surrounding blocks such as a register, energy can be minimized further. However energy minimization by voltage optimization is dependent on the system and the careful accounting of state elements versus logic offset the optimum voltage for minimum energy consumption towards sub-threshold operation.

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