

Christophe Giacomotto

Experience

Jan. 2006-Today Consulting Davis, CA

Independent Consultant

- VLSI: Worked for Integration corporation on standard cell performance optimization
- Web design: Re-designed an online shopping cart system (x-cart) from table to css based layout for WorkingManSoftware.com, created several small websites.

May 2004-Today University of California Davis, CA

Teaching Assistant, Electrical Engineering Dept.

- Undergraduate classes: Device Physics, Computer Architecture and Digital systems

Aug. 2001– April 2003 Fujitsu Processor Technology, Inc. San Jose, CA

Engineer, SPARC Microprocessor Research & Development Group

- 5 patents, met all company targets successfully, wrote over 20 research reports for the company.
- Contributed to the 20% performance improvement target from current circuit design techniques for over 7 research topics such as: active power stabilizer system, clock storage elements, novel repeater circuit and interconnect optimization, Logical Effort, domino logic noise and yield for modern floor planning techniques.
- Provided a thorough investigation on major trend induced problems such as rent's rule estimations, induction penalty, soft error rate, power consumption and yield vs. μ P floor planning and cache redundancy schemes.

Jan. 2001–April 2001 HAL Computer Systems Campbell, CA

Intern, Standard Cell design group

- Speed, power & noise sensitivity study analysis on Master-Slave latches.
- Designed a Latch library in Silicon-On-Insulator technology.

Education

May 2004–Now University of California Davis, CA

- Currently research assistant for Prof. Vojin G. Oklobdžija.
- Interests are in Custom VLSI circuit design with an emphasis on clocking systems.
- Built several Perl scripts to simulate large scale circuits such as adders, multipliers and registers with HSpice. These scripts enabled the analysis of digital circuits relative to energy and delay under various optimizations constrains (such as voltage, gain, slope, clock distribution, switching activity and internal device sizing).
- 2 publications on Clock Storage Elements and Ultra-Low-Voltage digital circuits

1998–2001 ESIEE (Ecole Superieure d'Ingenieurs) Paris, FRA

- MSc. in electronic engineering, participated in several training projects:
- Built an acceleration sensor (MEMS), used silicon membrane & piezoelectric effect.
- Designed, implemented and tested an FPGA to control the stability of a reverse pendulum.
- Fabricated circuits in Clean Room: Characterized MOS transistors and logic gates.

1996–1998

La Martiniere-Monplaisir

Cannes/Lyon, FRA

- Two-year advanced course in pure Mathematics, Physics and Mechanics to prepare competitive entrance exams to the French “Grandes Ecoles” (highly selective engineering institutes).
- 1996: Baccalaureat S equivalent to A-level. Specialized in Mathematics and Physics, passed with distinctions. (Stanislas, Cannes, France)

Skills

Software: Hspice, Cadence (composer), Matlab, Linpar, FrameMaker, 3DField.

Programming: PERL/Shell scripting, Verilog, HTML, basics in C/C++, Tcl & php

OS: Unix (HP/Solaris), Linux(Gentoo) & Microsoft (Dos/Windows).

Networking: Experience setting up GNU/Linux networks (NIS/NFS/Samba) for distributed scientific computation.

Language: Bilingual French/English

Patents & Publications

- **“Optimal inductor management”**
R. Masleid, C. Giacomotto, A. Harada. Jan. 2003, US Patent no. 6,906,579
 - **“Four-state switched decoupling capacitor system for active power stabilizer”**
C. Giacomotto, R. Masleid, A. Harada. Jan. 2003, US Patent no. 6,744,242
 - **“Complement reset multiplexer latch”**
R. Masleid, A. Harada, C. Giacomotto. Apr. 2003, US Patent no. 6,731,140
 - **“Complement reset latch”**
R. Masleid, C. Giacomotto. Apr. 2003, US Patent no. 6,577,176
 - **“Complement reset Buffer”**
R. Masleid, C. Giacomotto. Apr. 2003, US Patent no. 7,053,680
 - **“The Effect of the System Specification to the Optimal Choice of Clocked Storage Elements”**
N. Nedović, C. Giacomotto, V.G. Oklobdžija, Journal of Solid State Circuits, in press 2007
 - **“Energy-Delay Space Analysis for Clocked Storage Elements under Process Variations”**
C. Giacomotto, N. Nedović, V. G. Oklobdžija, 6th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), Montpellier, France Sept. 13-15, 2006
 - **“Logic Style Comparison for Ultra Low Power Applications”**
C. Giacomotto, V.G. Oklobdžija, Techcon (Semiconductor Research Corp.), Oct.24-26, 2005
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